IN THE SPECIFICATION

Please replace the paragraph beginning at page 9, line 3 with the following paragraph:

The ~~controller~~ interface 104 generally comprises a block (or circuit) 150, a block (or circuit) 152, a block (or circuit) 154 and a block (or circuit) 156. The circuit 150 may store address pointers in one or more control and/or status registers. The circuit 152 may be implemented as a memory interface state machine (to be described in more detail in connection with FIG. 2). The circuit 154 may be implemented as a bus interface unit. The circuit 156 may be implemented as a memory. In particular, the circuit 156 may be implemented as a bidirectional first in-first out (FIFO) memory. The interface 104 may be implemented with a variety of technologies (e.g., mask/field programmable logic devices). A data bus 160 may connect the memory interface state machine 152 with the FIFO 156. A data bus 162 may connect the memory 156 with the bus interface unit 154. A control bus 164 may connect the circuit 150, the circuit 152 and the circuit 154. A bus 166 may connect the circuit 152 with the memory 106. The data bus 160, the data bus 162, the control bus 164 and the bus 166 may be implemented as bi-directional busses.